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| **https://upload.wikimedia.org/wikipedia/commons/thumb/4/4e/VU_Logo.png/260px-VU_Logo.png** | **Advance Computer Architecture (CS501)**  Assignment # 02  **Spring 2024** | **Total Marks = 20 Deadline**  **Mon, Jun 24, 2024** |
| **Please carefully read the following instructions before attempting the assignment.**  **RULES FOR MARKING**  **It should be clear that your assignment would not get any credit if:**   * The assignment is submitted after the due date. * The submitted assignment does not open, or the file is corrupted. * Strict action will be taken if the submitted solution is copied from any other student or the Internet.   **You should consult the recommended books to clarify your concepts, as handouts are insufficient.**  **You are supposed to submit your assignment in Doc or Docx** **format.**  Any other formats like scanned images, PDF, ZIP, RAR, PPT, BMP, etc. will not be accepted.  **Topic Covered:**  The objective of this assignment is to assess the understanding of students about:   * CPU Polling Operations * I/O Subsystems * Direct Memory Address (DMA)   **Topics Covered**  Lecture # 12 to Lecture # 32 | | |
| **NOTE**  No assignment will be accepted *via email after the due date* (whether it is due to load shedding, internet malfunctioning, etc.). Hence, refrain from uploading assignments within the last hour of the deadline. It is recommended that the solution be uploaded at least two days before its closing date.  If you find any mistakes or confusion in the assignment (Question statement), please consult your instructor before the deadline. After the deadline, no queries will be entertained in this regard.  **For any query, feel free to email me at:**  [**CS501@vu.edu.pk**](mailto:CS501@vu.edu.pk) | | |

**Question Statement # 01**  **Total** **Marks (10)**

Consider a processor with a 950 MHz clock speed that requires 750 clock cycles to perform a context switch and start an Interrupt Service Routine (ISR). Each interrupt takes 11,000 cycles to execute the ISR, and the device generates 175 interrupt requests per second.

Additionally, the processor polls every 0.5 milliseconds when there are no interrupts, with each poll requiring 500 cycles.

Please answer the following questions:

1. How many processor cycles are spent per second managing device I/O (assuming interrupts are the sole method used)?
2. What percentage of CPU time is dedicated to interrupt handling for device I/O (based on the scenario in Part 1)?

Given:

* Clock speed = 950 MHz = 950 x 10^6 cycles/second
* Cycles to perform context switch and start ISR = 750 cycles
* Cycles to execute ISR = 11,000 cycles
* Interrupts per second = 175 interrupts

The total cycles per interrupt:

Total cycles per interrupt = 750 cycles + 11000 cycles = 11750 cycles

Total cycles per second for interrupts:

Total cycles per second = 11750 cycles/interrupt x 175 interrupts/second = 20556250 cycles per second

**Question Statement # 02**  **Total** **Marks (10)** Consider an Input/Output bus capable of transferring 16 bytes of data at a time. The designer intends to connect two devices to this bus:

1. A graphics card that requires a data transfer rate of 512 Megabytes per second. b. A sound card that requires a data transfer rate of 192 Megabytes per second.
2. Will this bus support smooth operation for both devices if its maximum frequency is limited to 100 MHz? Justify your answer.

Given

Bus width = 16 bytes

maximum bus frequency = 100 mhz

The maximum data transfer rate of bus:

Max transfer rate = 16 bytes x 100 mhz = 1600 megabytes/second

Required data transfer rates:

Graphics card: 512 Megabytes/second

Sound card: 192 Megabytes/second

Total required transfer rate:

Total required rate = 512 MB/s + 192 MB/s = 704 MB/s

**The End**